UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,515	09/28/2001	Tomoo Kimura	60188-101	2527

20277 7590 12/19/2005

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,515	KIMURA ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 9-12* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' amendment has been examined and remarks considered. Claims 1 and 3-11 are amended. Claims 1 and 3-12 are pending.

2. Applicants' amendment persuasively obviates the existing objections and rejections under 35 USC 112, second paragraph. The outstanding applicable rejections are incorporated herein.

Claim Objections

3. Claim 4 is objected to because of the following informalities: Pursuant to claim 4, at line 3, "condition verification" lacks sufficient antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Rejection of Claims 1, 3, 5, 6, 9, 11 and 12

6. **Claims 1, 3, 5, 6, 9, 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tani, U.S. Patent 5,471,409. Tani discloses a logic simulator apparatus and a circuit simulator apparatus capable of simulation based on signal propagation delay time. Tani does not explicitly disclose a current density analysis. However, Tani suggests current density analysis or calculation by inclusion of the elements required for a current density analysis. As outlined in section 4 of the Jerke et al. paper entitled "Hierarchical Current Density Verification for Electromigration Analysis in Arbitrarily Shaped Metallization Patterns of Analog Circuits", cited here for evidentiary purposes only and not as prior art, "Any current density calculation method requires at minimum (1) a set of current values as boundary constraints, (2) an appropriate representation of the layout geometry (3) technology dependent data and (4) specified application data (e.g. average chip temperature or a temperature field plot)". Tani includes all of the elements (listed in the Jerke paper) necessary for a current density calculation and furthermore discloses current calculating (col. 4, ll. 31-34). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention that Tani's current calculation includes or at least suggests the inclusion of current density calculation.

7. Pursuant to claim 1, which recites [a] circuit operation verifying method for verifying layout design specifications (col. 1, ll. 5-9) comprising loading condition

information as electrical specifications on voltages and currents applied to the circuit elements (col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66), circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21), and input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit operation simulation; simulating operation of the circuit to be verified while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time based on the loaded circuit diagram data and input patterns; *said simulating operation being performed at each of a plurality of specific times which are incrementally increasing* and storing the computed values in memory (col. 12, ll. 57-64); verifying that the circuit elements to be verified satisfy the loaded condition information using the stored voltage or current values (col. 5, ll. 3-17), said verification being performed after each simulating operation (col. 5, ll. 10-14); and calculating the next specific time by adding an infinitesimal time to the specific time after the verifying step (col. 12, ll. 43-56; col. 13, ll. 19-27), wherein the simulating step, the verifying step and the calculating step are performed repeatedly (Figures 6 and 9 illustrate iteration until the simulation is completed; the second preferred embodiment at columns 12-14 describe the iteration).

8. Pursuant to claim 3, wherein the condition information includes time specifications representing the frequency of violation against the electrical specification or the time period for which a violation state is allowable (col. 4, line 50 to col. 5, line 2), and whether or not the frequency of violation of the circuit elements being verified

satisfy the time specifications.(col. 4, line 30 to col. 5, line 14; see also col. 13, ll. 19-27; col. 14, ll. 37-55).

9. Pursuant to claim 5, wherein a verification period during which a condition verification is to be executed for the semiconductor circuit or a non-verification period during which no condition verification is to be executed is designated (col. 3, ll. 48-55; col. 4, ll. 55-59) and the condition verification is executed during the verification period.

10. Pursuant to claim 6, which recites a method for verifying that each of a number of circuit elements satisfies specifications (col. 1, ll. 5-9); loading condition information as electrical specifications on voltages and currents applied to circuit elements (col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66); circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21); input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit operation simulation with respect to time; simulating operation of the semiconductor circuit while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time (col. 11, ll. 9-18); verifying that circuit elements to be verified satisfy the specifications in the loaded condition information using the voltage values or the current values at the circuit elements stored in the memory (col. 5, ll. 3-17; col. 9, ll. 14-18; see also col. 9, ll. 3-8), said verification being performed concurrently (col. 5, ll. 10-14) with said simulating operation, wherein the specifications in the condition information are commonly designated for all the circuit elements of the semiconductor circuit being verified or

individually designated for the respective circuit elements (col. 2, line 50 to col. 3, line 33; see also col. 8, ll. 13-27).

11. Pursuant to claim 9, which recites a circuit operation verifying apparatus (Fig. 21; col. 1, ll. 10-13) for verifying that each of a number of circuit elements satisfies specifications (col. 1, ll. 5-9); loading means for loading condition information as electrical specifications on voltages and currents applied to circuit elements ((col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66); circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21); input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit simulation with respect to time; and operation simulation means for simulating operation of the semiconductor circuit while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time (col. 11, ll. 9-18); verification means for verifying that circuit elements to be verified satisfy the specifications in the loaded condition information using the voltage values or the current values at the circuit elements stored in the memory (col. 5, ll. 3-17; col. 9, ll. 14-18; see also col. 9, ll. 3-8), said verification means performing said verification concurrently (col. 5, ll. 10-14) with said simulation means performing said simulating operation, wherein the operation simulating means, the verifying means and the calculating means are performed repeatedly (Figures 6 and 9 illustrate iteration until the simulation is completed; the second preferred embodiment at columns 12-14 describe the iteration).

12. Pursuant to claim 11, which recites a circuit operation verifying apparatus (Fig. 21; col. 1, ll. 10-13) for verifying that each of a number of circuit elements satisfies specifications (col. 1, ll. 5-9); loading condition information as electrical specifications on voltages and currents applied to the circuit elements (col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66), circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21), and input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit operation simulation; simulating operation of the circuit to be verified while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time based on the loaded circuit diagram data and input patterns; storing the computed values, which are the result of the simulation step, in a memory after each simulating operation (col. 12, ll. 57-64); verifying that the circuit elements to be verified satisfy the loaded condition information using the stored voltage or current values, after each simulating operation (col. 5, ll. 3-17; see also col. 12, ll. 25-30), calculating the next specific time by adding an infinitesimal time to the specific time after the verifying step (col. 12, ll. 42-56; col. 13, ll. 12-31; col. 14, ll. 37-59).

13. Pursuant to claim 12, wherein the condition information includes electrical specifications representing current density values (col. 6, ll. 25-65) and heat generation amounts (col. 19, ll. 35-40) of the circuit elements, and the circuit diagram data of the semiconductor circuit to be verified includes layout information (col. 6, ll. 21-27), and current density analysis and heat generation analysis at positions inside the

semiconductor circuit to be verified are performed based on the current values at the circuit elements and the layout information stored in the memory (col. 6, line 63 to col. 7, line 2).

Rejection of claims 4 and 10

14. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tani, U.S. Patent 5,471,409 in view of Muraoka (JP2000-132578). Tani discloses a logic simulator apparatus and a circuit simulator apparatus capable of simulation based on signal propagation delay time. However, while Tani discloses the use of an apparatus, it does not disclose the use of a waveform display apparatus, although the display apparatus could be deemed to be within the scope of Tani's disclosure. Applicants' admitted prior art discloses the use of a display apparatus and it would have been obvious to one of ordinary skill in the art that the display apparatus disclosed by the prior art could be one embodiment of the apparatus disclosed in Tani for reporting results.

15. Pursuant to claim 4, wherein upon termination of the operation simulation and a condition verification of the semiconductor circuit, results of the condition verification are displayed on a waveform display apparatus displaying results of the simulation operation (see e.g. Muraoka translation ¶¶ 14, 18, 20-22) or a design apparatus used for circuit design or layout design of the semiconductor circuit (Tani, U.S. Patent 5,471,409; col. 5, ll. 10-12; col. 15, ll. 20-25).

16. Pursuant to claim 10, [a] circuit operation verifying apparatus (Fig. 21; col. 1, ll. 10-13) for verifying that each of a number of circuit elements satisfies specifications

(col. 1, ll. 5-9); loading means for loading condition information as electrical specifications on voltages and currents applied to circuit elements ((col. 2, line 50 to col. 3, line 33; col. 6, ll. 22-66); circuit diagram data representing connection information of the semiconductor circuit (col. 2, ll. 54-56; col. 8, ll. 13-21); input patterns of voltages (col. 2, line 66 to col. 3, line 2; col. 3, ll. 18-25) and currents (col. 3, ll. 10-13; col. 4, ll. 30-33) used for circuit simulation with respect to time; and operation simulation means for simulating operation of the semiconductor circuit while computing voltage values (col. 4, ll. 21-29) or current values (col. 4, ll. 30-46; col. 5, line 65 to col. 6, line 5) with respect to time (col. 11, ll. 9-18); verification means for verifying that circuit elements to be verified satisfy the specifications in the loaded condition information using the voltage values or the current values at the circuit elements stored in the memory (col. 5, ll. 3-17; col. 9, ll. 14-18; see also col. 9, ll. 3-8), said verification means performing said verification concurrently (col. 5, ll. 10-14) with said simulation means performing said simulating operation; waveform display means (see Muraoka translation ¶¶ 14, 18, 20-22); design means for circuit design (col. 6, ll. 20-26).

Allowable Subject Matter

17. Claims 7 and 8 contain allowable subject matter.

18. The following is a statement of reasons for the indication of allowable subject matter: In a circuit operation verifying method, the prior art does not teach or suggest a low-precision, high speed simulation to prepare circuit hierarchical information.

Remarks

19. Applicants' attempt to distinguish Tani by asserting that Tani is "NOT a verification performed dynamically with respect to each specific time as performed by the present invention." Nothing in Applicants' claim language emphasized anything about a verification being performed dynamically. But even if this were the case, Δt implies the existence of a dynamic calculation. Tani discloses a verification that is taking place in real-time, hence it is dynamic. The value of the time step is not what determines whether an operation is dynamic or static.

20. Tani does perform iteration of the steps, as shown in Figures 9, 15, and 25. Furthermore, why else would Tani maintain a time queue (see, e.g. col. 12, ll. 57-64), if the simulation was not iterative? Simulation is not a single event in time. Rather it continues in accordance with the signal change schedule at the input.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

23. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
Primary Examiner